IN THE CLAIMS

Amended claims follow. Insertions are underlined, while deletions are struck out. The status of each claim is included prior to each heading.

1. (Currently Amended) An integrated circuit, comprising:

an active circuit;

a metal layer disposed, at least partially, above the active circuit; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer defines a frame;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the frame ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the frame ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

2. (Original) The integrated circuit as recited in claim 1, wherein the active circuit includes an input/output (I/O) bus.

3. (Cancelled)

4. (Original) The integrated circuit as recited in claim 1, wherein the metal layer includes an interconnect metal layer.

5. (Original) The integrated circuit as recited in claim 4, wherein the interconnect metal layer interconnects the bond pad with a plurality of underlying metal layers.

6. (Previously Presented) The integrated circuit as recited in claim 5, wherein each of the underlying metal layers is in electrical communication by way of a plurality of vias.

7. (Original) The integrated circuit as recited in claim 1, wherein the frame defines an outer periphery and an inner periphery.

8. (Original) The integrated circuit as recited in claim 7, wherein the frame is enclosed.

9. (Original) The integrated circuit as recited in claim 7, wherein the metal layer defines an island formed within and spaced from the inner periphery of the frame of the metal layer.

10. (Original) The integrated circuit as recited in claim 9, wherein the island of the metal layer includes a plurality of openings formed therein.

11. (Original) The integrated circuit as recited in claim 10, wherein the openings are adapted for facilitating an interlock between the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

12. (Original) The integrated circuit as recited in claim 10, wherein the openings are completely enclosed around a periphery thereof.

13. (Original) The integrated circuit as recited in claim 10, wherein the openings have a substantially square configuration.

14. (Original) The integrated circuit as recited in claim 1, wherein a plurality of interconnect vias are formed along the frame.

15. (Cancelled)

16. (Currently Amended) An integrated circuit, comprising:

an active circuit means for processing electrical signals;

a metal layer disposed, at least partially, above the active circuit means and including a frame means for preventing damage incurred during a bonding process; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit means;

wherein the frame means ensures that bonds are capable of being placed over the active circuit means without damage thereto during a bonding process;

wherein the active circuit means includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the frame means ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

17. (Currently Amended) An integrated circuit, comprising:

a semiconductor structure including an active circuit including an input/output (I/O) bus and a plurality of transistors forming a core of circuits;

a plurality of vertically spaced underlying metal layers disposed, at least partially, under the active circuit and around a periphery thereof, wherein each of the underlying metal layers are in electrical communication by way of a plurality of underlying vias with the active circuit and other underlying metal layers;

an interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit and around a periphery thereof, the interconnect metal layer being in electrical communication with the underlying metal layers by way of a plurality of additional vias, wherein the interconnect metal layer defines a frame with an outer periphery and an inner periphery;

an inter-metal dielectric layer disposed, at least partially, above the interconnect metal layer, the inter-metal dielectric layer constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material;

a top metal layer disposed, at least partially, above the inter-metal dielectric layer, the top metal layer for serving as a bond pad, the top metal layer being in electrical

communication with the interconnect metal layer by way of a plurality of interconnect vias; and

a passivation layer disposed, at least partially, above the top metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the frame ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process;

wherein an entirety of at least one of the transistors is disposed directly below the bond pad, and the frame ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

18. (Currently Amended) An integrated circuit, comprising:

an active circuit;

a metal layer disposed, at least partially, above the active circuit, the metal layer defining a substantially enclosed, rectangular frame with an outer periphery and an inner periphery;

a dielectric layer disposed, at least partially, above the metal layer; and

a bond pad disposed, at least partially, above the metal layer;

wherein a plurality of vias are formed along the frame for electrical communication between the metal layer and the bond pad;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the frame ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the frame ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Previously Presented) The integrated circuit as recited in claim 1, wherein the metal layer is disposed, at least partially, above the active circuit along a vertical axis.

25. (Cancelled)

26. (Previously Presented) The integrated circuit as recited in claim 11, wherein the inter-metal dielectric layer is constructed from a low-K dielectric material.

27. (Previously Presented) The integrated circuit as recited in claim 11, wherein the inter-metal dielectric layer is constructed from a fluorinated silica glass (FSG) material.

28. (Cancelled)

29. (Previously Presented) The integrated circuit as recited in claim 9, wherein the island is spaced from the frame with a continuous, uninterrupted space therebetween.

30. (Previously Presented) The integrated circuit as recited in claim 7, wherein the inner periphery of the frame is continuous and defines a single, central rectangular space.